

Notice of References Cited

Application/Control No.

09/405,618

Applicant(s)/Patent Under
Reexamination
BLOMGREN ET AL.

Examiner

Dwin M Craig

Art Unit

2123

Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6289497 ✓	09-2001	Leight et al.	716/17
	B	US-5706476 ✓	01-1998	Giramma	703/15
	C	US-5051941 ✓	09-1991	Takamine et al.	703/15
	D	US-5960188 ✓	09-1999	Linke et al.	703/14
	E	US-5884065 ✓	03-1999	Takasaki	703/14
	F	US-4675832 ✓	06-1987	Robinson et al.	345/441
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
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	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	"IEEE Standard Multivalued Logic System for VHDL Model Interoperability (Std_logic_1164)", March 18, 1993, The Institute of Electrical and Electronics Engineers, Inc. New York, N.Y.; ISBN 1-55937-299-0. ✓
	V	C. Rozon "On the Use of VHDL as a Multi-Valued Logic Simulator", IEEE 1996, Pages 110-115. ✓
	W	
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*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

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